WHAT IS CLAIMED IS:

1. An integrated circuit having two respective decode/selection circuits respectively located along opposite edges of a three-dimensional memory array for selecting wordlines or bitlines which respectively exit the memory array along said opposite edges.

2. The integrated circuit as recited in claim 1 wherein half of said wordlines or bitlines respectively exit the memory array along each of said opposite edges.

3. The integrated circuit as recited in claim 1 wherein at least a portion of the two decode/selection circuits are disposed in a substrate upon which the memory array is formed.

4. The integrated circuit as recited in claim 3 wherein at least a portion of the two decode/selection circuits are folded beneath the memory array.

5. The integrated circuit as recited in claim 1 wherein the two respective decode/selection circuits comprise respective row circuits for respectively selecting one or more wordlines respectively exiting on east and west edges of the memory array, and wherein half of said wordlines respectively exit the memory array along each of said east and west edges.

6. The integrated circuit as recited in claim 5 wherein each of the two row circuits is configured, when selected, to simultaneously select more than one wordline within a single row of wordlines.

7. The integrated circuit as recited in claim 6 wherein the simultaneously selected more than one wordline within a single row of wordlines comprises a respective wordline on each of at least two wordline layers of the memory array.

8. The integrated circuit as recited in claim 5 further comprising two respective column circuits for respectively selecting one or more bitlines respectively exiting along

north and south edges of the memory array, and wherein half of said bitlines respectively exit the memory array along each of said north and south edges.

9. The integrated circuit as recited in claim 8 wherein at least a portion of both row circuits and at least a portion of both column circuits are disposed in a substrate upon which the memory array is formed, and wherein both row circuits and/or both column circuits are at least partially folded beneath the memory array.

10. The integrated circuit as recited in claim 1 wherein the memory array comprises non-volatile memory cells.

11. The integrated circuit as recited in claim 10 wherein the memory array comprises passive element memory cells.

12. The integrated circuit as recited in claim 11 wherein the memory array comprises anti-fuse memory cells.

13. An integrated circuit comprising:

a three-dimensional memory array having at least two planes of memory cells formed above substrate;

a first decode/selection circuit having outputs associated with wordlines or bitlines which exit on one edge of the memory array; and

a second decode/selection circuit having outputs associated with wordlines or bitlines which exit on another edge opposite the one edge of the memory array.

14. The integrated circuit as recited in claim 13 wherein the first and second decode/selection circuits are disposed at least partially beneath the memory array.

15. The integrated circuit as recited in claim 13 wherein the first and second decode/selection circuits respectively comprise:

a first row selection circuit disposed at least partially beneath the memory array having outputs along a west edge of the memory array and associated with wordlines; and

a second row selection circuit disposed at least partially beneath the memory array having outputs associated with wordlines exiting on an east edge of the memory array.

16. The integrated circuit as recited in claim 15 comprising first and second row selection circuit outputs that are coupled to respectively drive a respective wordline on at least one wordline layer within a row of wordlines.

17. The integrated circuit as recited in claim 16 comprising first and second row selection circuit outputs that are coupled to respectively drive a wordline on each of at least two wordline layers within the same row of wordlines.

18. The integrated circuit as recited in claim 16 wherein:
the wordlines of each row are grouped into first and second sets; and
a given output of the first and second row selection circuits is respectively coupled to simultaneously drive either the first or second set of wordlines within a respective row of wordlines.

19. The integrated circuit as recited in claim 18 wherein the first and second sets of wordlines within each row of wordlines each includes only one wordline.

20. The integrated circuit as recited in claim 18 wherein the memory array includes at least four wordline layers and the first and second sets of wordlines within each row of wordlines each includes a wordline on each of at least two wordline layers.

21. The integrated circuit as recited in claim 15 comprising first and second row selection circuit outputs which each connect to a respective wordline on each of at least two wordline layers.

22. The integrated circuit as recited in claim 15 wherein the memory array comprises wordlines on a given wordline layer associated with a first plane of memory cells above the given wordline layer and also associated with a second plane of memory cells below the given wordline layer.

23. The integrated circuit as recited in claim 15 comprising wordlines on at least two wordline layers that are of unequal length and having staggered contact structures to respective row selection circuit outputs.

24. The integrated circuit as recited in claim 13 wherein the memory array comprises non-volatile memory cells.

25. The integrated circuit as recited in claim 24 wherein the memory array comprises field-programmable memory cells.

26. The integrated circuit as recited in claim 25 wherein the memory array comprises one-time-programmable memory cells.

27. The integrated circuit as recited in claim 25 wherein the memory array comprises write/erase/rewrite memory cells.

28. The integrated circuit as recited in claim 24 wherein the memory array comprises passive element memory cells.

29. The integrated circuit as recited in claim 28 wherein the memory array comprises anti-fuse memory cells.

30. The integrated circuit as recited in claim 28 wherein the memory array comprises fuse memory cells.

31. The integrated circuit as recited in claim 24 wherein the memory array comprises memory cells which are programmable during manufacture.

32. The integrated circuit as recited in claim 13 wherein the first and second decode/selection circuits are formed entirely in the substrate.

33. The integrated circuit as recited in claim 13 wherein the first and second decode/selection circuits comprise driver circuits that are formed above the substrate using materials common to the memory array.

34. The integrated circuit as recited in claim 13 wherein at least a portion of the first and second decode/selection circuits are folded beneath the memory array.

35. The integrated circuit as recited in claim 15 further comprising:

a first column selection circuit disposed at least partially beneath the memory array having outputs along a north edge of the memory array and associated with bitlines; and

a second column selection circuit disposed at least partially beneath the memory array having outputs along a south edge of the memory array and associated with bitlines.

36. The integrated circuit as recited in claim 35 wherein the memory array comprises multiple sub-arrays, each including one or both of dual opposing row selection circuits and dual opposing column selection circuits.

37. An integrated circuit comprising:

a three-dimensional memory array having at least two planes of memory cells formed above substrate, said array including respective rows of wordlines on at least two wordline layers;

a first row selection circuit disposed at least partially beneath the memory array and having outputs along an east side of the memory array and associated with wordlines which exit the memory array to the east side thereof;

a second row selection circuit disposed at least partially beneath the memory array and having outputs along a west side of the memory array and associated with wordlines which exit the memory array to the west side thereof;

a first column selection circuit disposed at least partially beneath the memory array and having outputs along a north side of the memory array and associated with bitlines which exit the memory array to the north side thereof; and

a second column selection circuit disposed at least partially beneath the memory array and having outputs along a south side of the memory array and associated with bitlines which exit the memory array to the south side thereof.

38. The integrated circuit as recited in claim 37 wherein:

the wordlines of each row are grouped into multiple sets, each numbering at least one wordline; and

a given output of the first and second row selection circuits is respectively coupled, when selected, to simultaneously drive each wordline within a set of wordlines within a respective row of wordlines.

39. The integrated circuit as recited in claim 38 wherein the first and second row selection circuits respectively comprise:

a row address decoder circuit having a plurality of output nodes, each corresponding to a row of wordlines in the memory array; and

a respective plurality of set select devices responsive to a respective row address decoder output node, each of the plurality of set select devices also responsive to an associated set select signal for driving an associated set of wordlines disposed on one or more wordlines layers.

40. The integrated circuit as recited in claim 39 wherein each set of wordlines includes a respective wordline on half of the wordline layers within a row of wordlines.

41. The integrated circuit as recited in claim 38 wherein each set of wordlines within each row of wordlines each consists of only one wordline.

42. The integrated circuit as recited in claim 39 wherein the memory array comprises:

wordlines on a given wordline layer associated with a first plane of memory cells above the wordline layer and also associated with a second plane of memory cells below the given wordline layer, and

non-volatile anti-fuse memory cells.

43. The integrated circuit as recited in claim 39 further comprising wordlines on at least two wordline layers that are of unequal length and having staggered contact structures to associated select devices disposed in the substrate.

44. The integrated circuit as recited in claim 37 wherein the memory array comprises multiple sub-arrays, each including one or both of dual opposing row selection circuits and dual opposing column selection circuits.